Hardware Support for Fine-Grain Multi-Threading in LEON3

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Abstract— The article describes instruction set extensions for a variant of multi-threading called micro-threading for the LEON3 SPARCv8 processor. An architecture of the developed processor ispresented and its key blocks described - cache controller, register file, thread scheduler. The processor has been implemented in a Xilinx Virtex2Pro and Virtex5 FPGAs. The extensions are evaluated in terms of extra resources needed, and the overall performance of the developed processor is shown for a simple DSP computation typical for embedded systems.

REFERENCES

[1] T. Takayanagi, J. L. Shin, B. Petrick, J. Su, and A. S. Leon, "A dual-core 64b ultrasparc microprocessor for dense server applica- tions," in *DAC*, S. Malik, L. Fix, and A. B. Kahng, Eds. ACM, 2004, pp. 673–677.

[2] P. Kongentira, K. Aingaran, and K. Olukotum, "Niagara: a 32-way multithreaded SPARC processor," *IEEE Micro*, vol. 25, no. 2, pp. 21–29, 2005.

[3] K. D. Kissell, "MIPS MT: A multithreaded RISC architecture for embedded real-time processing," in *HiPEAC*, ser. Lecture Notes in Computer Science, P. Stenström, M. Dubois, M. Katevenis, R. Gupta, and T. Ungerer, Eds., vol. 4917. Springer, 2008, pp. 9–21.

[4] J. Gaisler, E. Catovic, and S. Habinc, *GRLIB IP Library User's Manual*. Gaisler Research, 2007.

[5] T. Ungerer, B. Robič, and J. Šilc, "A survey of processors with explicit multithreading," *ACM Comput. Surv.*, vol. 35, no. 1, pp. 29–63, 2003.

[6] C. R. Jesshope and B. Luo, "Micro-threading: A new approach to future RISC." in *Proceedings of the 5th Australasian Computer Architecture Conference*. IEEE Computer Society press, 2000, pp. 34–41.

[7] C. Jesshope, "Scalable instruction-level parallelism," in *Computer Systems: Architectures, Modeling, and Simulation*. Springer Berlin / Heidelberg, 2004, pp. 383–392.

[8] C. R. Jesshope, "muTC - an intermediate language for program- ming chip multiprocessors," in *Asia-Pacific Computer Systems Architecture Conference*, 2006, pp. 147–160.

[9] Arvind and R. S. Nikhil, "Executing a program on the MIT tagged-token dataflow architecture," *IEEE Transaction on Computers*, vol. 39, no. 6, pp. 300–318, 1990.

[10] J. Sykora, L. Kafka, M. Danek, and L. Kohout, "Microthreading as a novel method for close coupling of custom hardware accelerators to SVP processors," in *Proceedings of the 14th EUROMICRO Conference on Digital System Design (DSD2011)*. Conference Publishing Services, 2011.

[11] M. Danek, L. Kafka, L. Kohout, and J. Sykora, "Instruction set extensions for multi-threading in LEON3," pp. 237–242.

[12] J. Sykora, L. Kafka, M. Danek, and L. Kohout, "Analysis of ex- ecution efficiency in the microthreaded processor UTLEON3," in *Proceedings of the 2011 Conference on Architecture of Computing Systems (ARCS 2011)*, ser. Lecture Notes in Computer Science, vol. 6566. Springer, 2011, pp. 110–121.

[13] Sun Microsystems. RAMP retreat August, 2008 update. http://www.opensparc.net/publications/presentations/ramp-retreat- august-2008-update.html.

[14] C. R. Jesshope, J.-M. Philippe, and M. van Tol, "An architecture and protocol for the management of resources in ubiquitous and heterogeneous systems based on the svp model of concurrency," in *SAMOS*, ser. Lecture Notes in Computer Science, M. Berekovic, N. J. Dimopoulos, and S. Wong, Eds., vol. 5114. Springer, 2008, pp. 218–228.

[15] The Apple-CORE Consortium. Architecture Paradigms and Programming Languages for Efficient programming of multiple COREs. http://www.apple-core.info.