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Low Power Full Adder Design Using PTM Transistor Model

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***Abstract*—At present the processing power of the digital electronic chip is enormous and that has been possible because of the continuous improvement of the design methodology and fabrication technology. So, the data processing capability of the chip is increased significantly. Data processing in the electronic chip means the arithmetic operation on that data. For that reason, ALU is present in any processor. Full adder is one of the critical components of arithmetic unit. Improvement of the full adder is necessary for improving the computational performance of a chip. In order to design an efficient full adder, designer should choose an appropriate logic style. In this research, two new model of full-adder circuits are designed and analyzed using Pass Transistor logic in order to reduce power consumption and increase operational speed. The first proposed adder consists of 8 transistors and the second one consists of 10 transistors. LTSPICE is employed for simulating the proposed circuits using16nm low power high-k strained silicon transistor model. The overall performance of the proposed adder circuits and comparative results demonstrate the superiority of the proposed model.**

Keywords—ALU, Complementary Pass Logic, PTM strained Silicon model, Power-Delay Product, FINFET, and CNTFET

I. INTRODUCTION

According to the 'Moore's law, the performance of a VLSI circuit is doubling every 18 months. In order to keep the performance rate according to this law is not possible by improving the fabrication technology. Therefore, suitable circuit design is very much necessary for achieving the high-performance goal. The performance of a microprocessor is increasing day by day. Switching frequency & power consumption of a microprocessor has significantly improved over past 10 years. ALU is the vital element of a microprocessor.

Adder circuit is one of the basic components of ALU. It is also the building block of subtraction, and multiplication circuits. An efficient adder design has an impact on the performance of ALU and the microprocessor. Therefore, designing high speed, low-power, and full-swing output full - swing output full adder has become a vital concern in VLSI circuits and systems design [6]. Now-a-days, designers are trying to reduce power consumption of the VLSI circuit. The major components of power consumption are switching power & short circuit power.

Enormous research papers have been published regarding the design of full adder circuit based on various logic styles. Although all of them present a cell that performs the same function, but the method of implementing and device counts are varied. Static CMOS full adder is a classical one which uses only one logic style for the entire circuit, i.e., using pull-up PMOS transistors and pull-down NMOS transistors to implement final outputs. The layout of the CMOS is less complex and efficient due to complementary pairs but there is some drawback. In this type, large number of transistors (28T) is required as a result the area is increased [4]. The other classical full adder is Complementary Pass Logic (CPL) full adder containing NMOS pass transistors and pull-up PMOS transistors to provide swing restoration. Both types of designs have full-swing outputs, simple and symmetrical layout, but huge number of transistors is required (32T). And also, these circuits need large amount of power are die area [5]. Another problem of CPL is the signal degradation when the signal is passed through a series of transistors.

In order to achieve compactness and low power consumption, it is highly in demand to reduce the number of transistors. Pass Transistor Logic (PTL) is employed to reduce the transistor count as well as power dissipation [3]. Although, voltage drop is the main drawback of PTL as logic '1' passing through NMOS transistor is never be equal to the V_{DD} and logic '0' is never be equal to the GND. But in a processor, there are so many arithmetic units and a large number of adder circuits are needed to be designed in a very limited area [3]. So, the PTL is still in demand for low power IC design. Several researchers have proposed full-adder circuit designed with significantly a smaller number of transistors such as: 8T and 10T [11-17]. However, their model consumes more power and take longer time to response.

In this research, two full-adder circuits are proposed and both are implemented using PTL. First full-adder is designed using only 8 transistors (8T) and the other one consists of 10 transistors (10T). Though the proposed model also requires the same number of transistors as other research group [11-17], but the arrangement of the transistors is very different from their circuit. Extensive simulation experiments are

carried out by employing predictive technology model (PTM) [10]. Transistor of 16nm low power high-k strained silicon model is used to measure different parameters. Strained silicon is a layer which is epitaxially grown on the gate of a MOSFET to improve mobility. Comparative results demonstrate the suitability and competency of the proposed circuits. In the next section, the proposed models are discussed in detail. Section III describes the simulation results and different parameters are calculated in section IV. Comparative analysis is presented in section V and the concluding remarks are discussed in section VII.

II. PROPOSED FULL ADDER CIRCUITS

Two new full-adder circuits are designed and both of them are based on pass transistor logic in order to reduce the number of transistors. Design goal is to reduce the area, time delay and high-speed operation.

A. Proposed 8T Adder

The proposed 8T full-adder circuit is shown in figure 1. The special characteristic of this circuit is that the carry unit is designed with only 2 NMOS transistors. So, the number of transistor count is less and the power dissipation of this adder becomes significantly low. 3T XOR gate configuration is realized and used to design sum module.

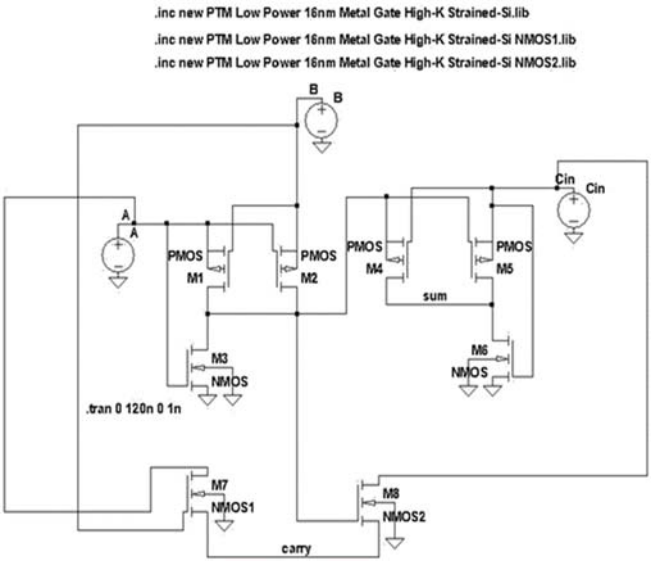

Figure 1: Proposed 8T Full Adder

Operation: The upper 6 transistors (4 PMOS and 2 NMOS) generate sum and the lower 2 NMOS generate carry. The adder which shows in figure 1 is designed using the following sum and carry equations

$$\text{Sum} = (A \oplus B) \oplus C_{in} \quad (1)$$

$$\text{Carry} = \{(A \oplus B) * C_{in}\} + (A * B) \quad (2)$$

Here we explain how the schematic in figure 1 follow the equation 1 and 2. Refer to figure 1, the M1, M2 and M3 transistors act as a XOR gate. Signal A and B are placed in the source of M1 and M2. We get the output A⊕B at the common drain of M1 and M2. Similarly, M4, M5 and M6 transistors also act as a XOR gate. The output from the first XOR gate (A⊕B) and the signal C_{in} are placed in the source of M4 and M5. The output of the 2nd XOR gate (M4, M5 and M6) is A⊕B⊕C_{in}. we get that output at the common drain of M4 and M5. That is the sum of the adder which is written in equation 1.

Now the lower 2 transistors basically act as individual AND gate. The output from 1st XOR gate are placed in the drain of the M8 transistor and signal C_{in} is placed in the gate of M8 transistor. So theoretically we get (A⊕B)*C_{in} at the source of M8. Similarly, signal A and B are placed in the gate and drain respectively of the M7 transistor. Then we get (A*B) at the source of M7. As the source of M7 and M8 are connected (Figure 1) according to TG logic we get {(A ⊕B)*C_{in} +(A*B)} at the common source of M7 and M8. That is the carry of the adder which is written in equation 2.

A theoretical explanation is given to understand the operation of our proposed circuit. we know that the equation of the drain to source current of MOSFET is $I_{ds} = \mu C_{ox}(W/L)(V_{gs}-V_t-(V_{ds}/2))V_{ds}$ in linear region. But in VLSI application the MOSFET act as a switch so we need to operate the MOS in saturation region. In saturation region, the drain to source current equation is $I_{ds} = \frac{1}{2}\mu C_{ox}(W/L)(V_{gs}-V_t)^2$ Threshold voltage V_t is process dependent i.e. it has a fixed value for a particular FET. If it is fixed then the drain to source current depends only on the geometry i.e. W/L ratio of MOSFET. If W/L ratio is greater than 1 then the I_{ds} will be higher and if W/L ratio is less than 1 then the I_{ds} will be lower. At that point, if we carefully look at the proposed adder circuit, it is seen that 3T XOR configuration is used. The drawback in this configuration is that, if both the PMOS becomes logic '1', then the output will be floating. In order to compensate this problem, an NMOS transistor is introduced in such a manner so that, the output becomes logic '0' as desired for XOR operation. But another problem is arisen as the other outputs of XORs are severely degraded. So, the transistors are weakened by changing the W/L ratio. As a result, we get our desirable output as well as less degradation of the output. The advantage of this technique is less current and less static power dissipation in the circuit. Few other parameters of the model are also changed to obtain desired result. Rest of the parameters of the model file are unchanged. All the transistors are separately designed for both sum and carry unit and included in those transistors SPICE models. Table I shows the changed parameters list.

TABLE I. MODIFIED PARAMETERS* (8T ADDER)

Sum unit			**Carry unit**		
PMOS	***Parameter***	***Modified value***	NMOS1 (M7) & NMOS2 (M8)	***Parameter***	***Modified value***
	W_{int}	$5e^{-10}$		W_{int} (M8)	$5e^{-11}$
				n_{dep}	$1e^{26}$
				n_{SD}	$9e^{30}$
				r_{dsw} (M7)	3500
NMOS	W_{int}	$5e^{-13}$		r_{dsw} (M8)	$1e^{-4}$
				W_{int} (M7)	$5e^{-13}$
				V_{tho} (M7) & V_{tho} (M8)	0.19191 & 0.59191

*Note: the name of the modified parameters is given below

W_{int}= width offset fitting parameter from I-V without bias

n_{dep}= Channel doping concentration at depletion edge for zero body bias

n_{SD}= Source/drain doping concentration

r_{dsw}= parasitic source to drain resistance per unit width

V_{tho}= threshold voltage for a long channel device at V_{bs}=0 and small V_{ds}

B. Proposed 10T Adder

This is another proposed adder circuit. This is also based on PTL and designed using 10 transistors. Figure 2 shows the schematic of our proposed 10T full adder.

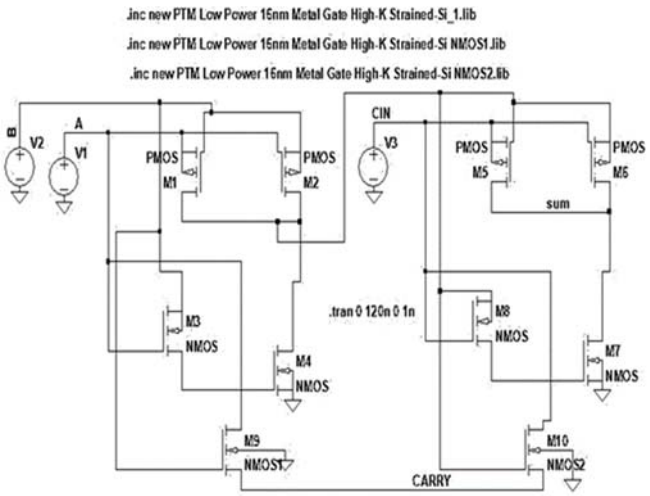

Figure 2: Proposed 10T Full Adder

Operation: The upper 8T (4 PMOS and 4 NMOS) generate sum and the lower 2 NMOS generate carry. This circuit is also designed using Equation 1 & 2.

Here 4T XOR configuration is used to generate sum module. In previous section it is discussed about the problems and complexity of 3T XOR configuration. In order to overcome those drawbacks, 4T XOR configuration is proposed here for obtaining better performance.

Again, we explain how the schematic in figure 2 follow the equation 1 and 2. Refer to figure 2, the M1, M2, M3 and M4 transistors act as a XOR gate. Signal A and B are placed in the source of M1 and M2. We get the output A⊕B at the common drain of M1 and M2. Similarly, M5, M6, M7 and M8 transistors also act as a XOR gate. The output from the first XOR gate (A⊕B) and the signal C_{in} are placed in the source of M5 and M6. The output of the 2nd XOR gate (M5, M6, M7, M8) is A⊕B⊕C_{in}. we get that output at the common drain of M5 and M6. That is the sum of the adder which is written in equation 1.

Carry generation technique is similar to schematic 1. (A⊕B)*C_{in} comes from M10 and (A*B) comes from M9. The final output comes from the common source of M9 and M10 labeled as 'CARRY' in figure 2.

The parameters of the model file are shown in Table II.

TABLE II. MODIFIED PARAMETERS* (10T ADDER)

Sum unit			Carry unit		
	Parameter	***Modified value***		***Parameter***	***Modified value***
PMOS	W_{int}	Unchanged	NMOS 1 (M9) & NMOS 2 (M10)	W_{int} (M10)	$5e^{-11}$
				n_{dep}	$1e^{26}$
				n_{SD}	$9e^{30}$
				r_{dsw} (M9)	3500
NMOS	W_{int}	$5e^{-13}$		r_{dsw} (M10)	$1e^{-4}$
				W_{int} (M9)	$5e^{-13}$
				V_{tho} (M9) & V_{tho} (M10)	0.19191 & 0.59191

III. SIMULATION RESULT

Both the proposed adder circuits (figure 1 and 2) are simulated in order to measure some circuit parameters which evaluates the overall performance of the design. LTSPICE software is used for simulating. The simulation is carried out using 16nm PTM model with power supply of 0.9v at frequency 25MHz. The input signal which is used for simulation of proposed adder are shown in Figure 3 and the output responses of two proposed adder are shown in figure 4 and 5 respectively (only first 3 cycles are shown).

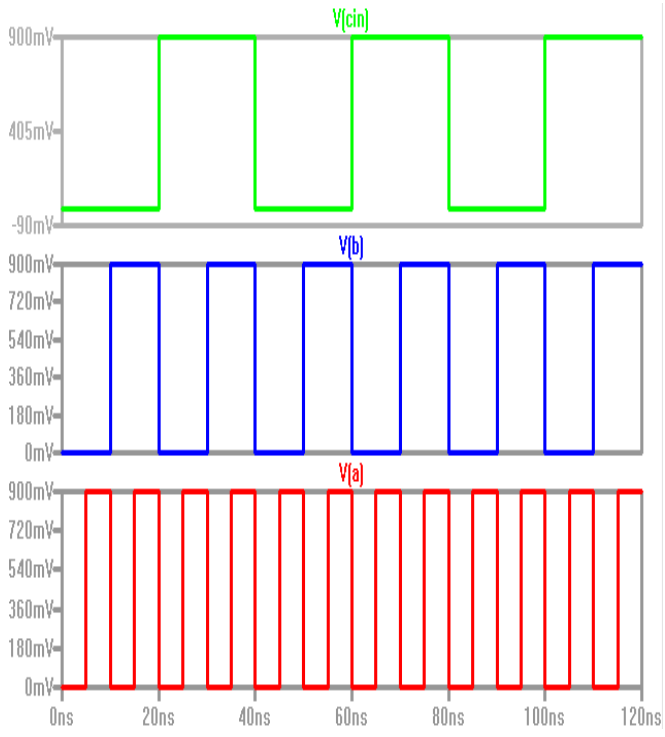

Figure 3: Input signals ($C_{in,}$ B and A)

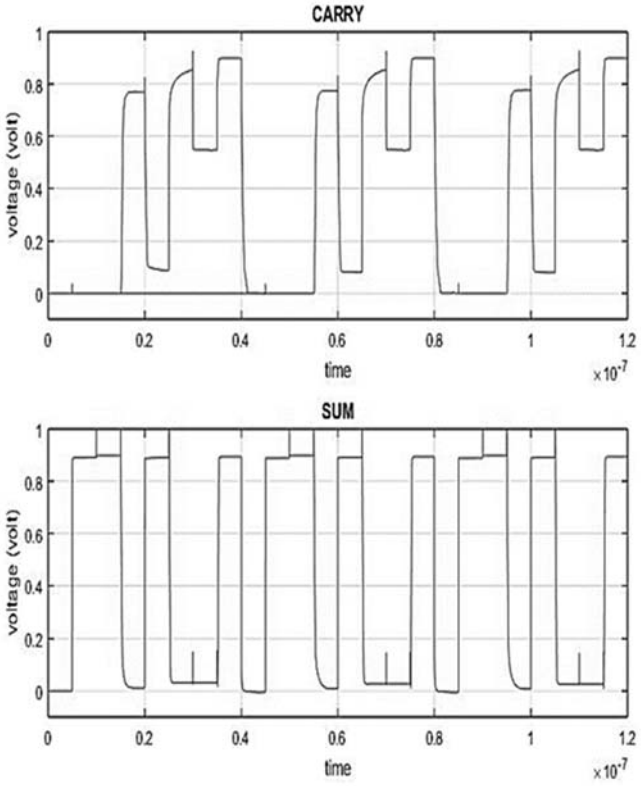

Figure 4: Output response of Proposed 8T Adder

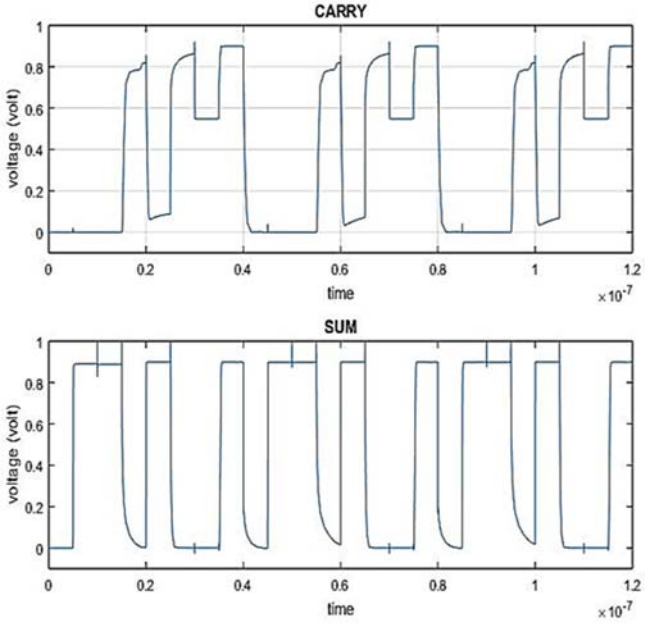

Figure 5: Output response of proposed 10T adder

IV. PARAMETER CALCULATION

In order to analysis the performance of any digital circuit, we need to calculate few parameters of that circuit. After calculating the parameters, that should compare with another existing circuit parameters where the existing circuit and the proposed circuit do the same job. In this case we calculated the average power consumption, delay for carry, delay for sum, total delay and power delay product for both the proposed circuits. The calculated value of the defined parameters is shown in Table III and IV.

TABLE III. MEASURED PARAMETERS OF PROPOSED 8T ADDER

1	Average power consumption (nW)	2.09
2	Average delay for carry(s)	2.11e-10
3	Average delay for sum(s)	9.12e-11
4	Total average delay(s)	1.51e-10
5	PDP (nW. s)	3.16e-19

TABLE IV. MEASURED PARAMETERS OF PROPOSED 10T ADDER

1	Average power consumption (nW)	1.21
2	Average delay for carry(s)	2.39e-10
3	Average delay for sum(s)	8.07e-11
4	Total average delay(s)	1.59e-10
5	PDP (nW. s)	1.95e-19

V. COMPARISON OF MEASURED PARAMETERS

The aim of a designer is that the designed product must be better than previous. In this section performance of the proposed adder circuits are compared with some existing another adder circuit in order to evaluate the competency of the proposed circuits.

The proposed adder circuits are compared with Deepa, Sampath 6T adder [3] and Reddy, Kavita 6T adder [2]. A comparison table of the measured parameters is given in Table V.

TABLE V. PERFORMANCE COMPARISON OF ALL ADDERS

Full Adder	*Average power (nW)*	*Average delay (carry) (s)*	*Average delay (sum) (s)*	*Total average delay (s)*	*PDP (nW. s)*
Proposed 8T adder	2.09	2.11e-10	9.12e-11	1.51e-10	3.16e-19
Proposed 10T adder	1.21	2.39e-10	8.07e-11	1.59e-10	1.95e-19
Deepa, Sampath adder [3]	3.56	1.21e-10	1.45e-10	1.33e-10	4.75e-19
Reddy, Kavita adder [2]	4.28	6.92e-11	8.56e-11	7.74e-11	3.32e-19

The bar graph is also added for the better understanding. The comparison of power, total delay, and PDP of all adders are presented in bar diagram in Fig. 6, Fig. 7 and Fig. 8.

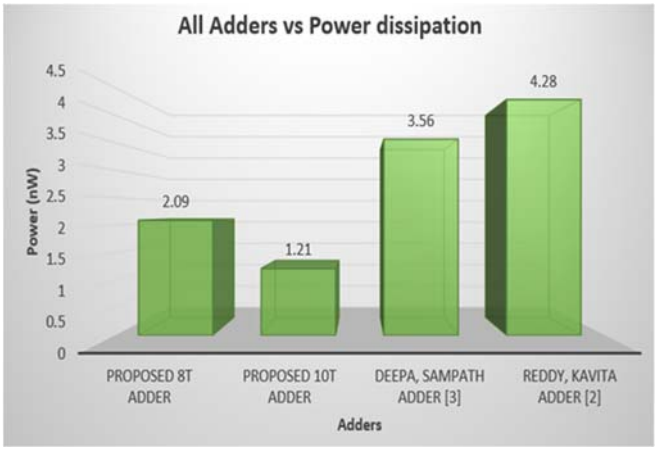

Figure 6: Comparison of the power consumption of all adders

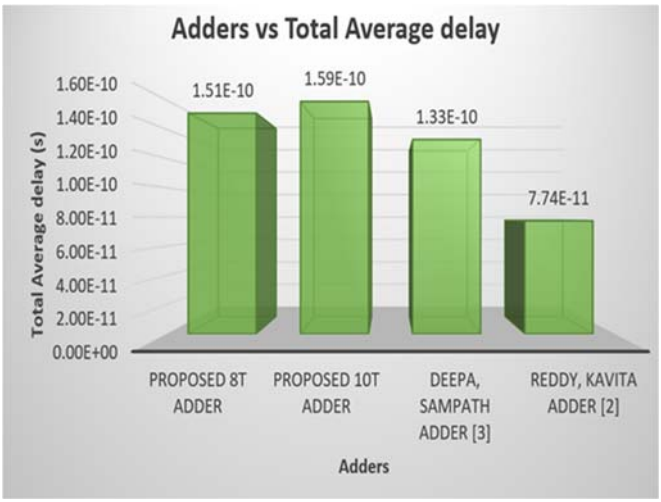

Figure 7: Comparison of the total average delay of all adders

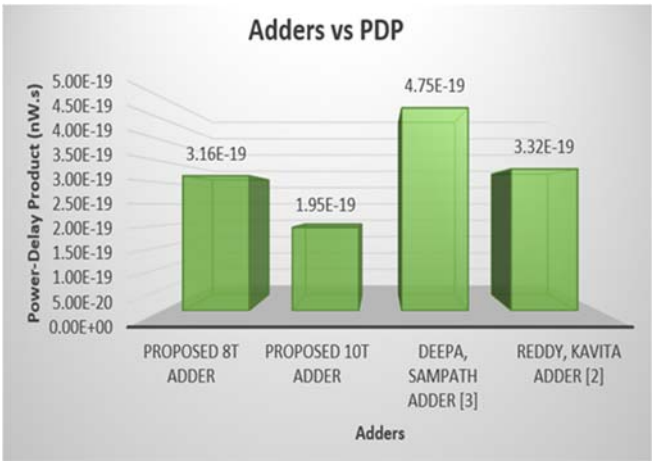

Figure 8: Comparison of the PDP of all adders

VI. DISCUSSION

In the previous section, our proposed adders are compared with two different adders and the both adders are designed using only 6 transistors [3,2]. But the truth is that both adders are applicable if the inputs and inverted inputs are available.

However, in order to get inverted input, one must need to use an inverter. And an inverter is made out of two transistors. So basically, they are not truly 6T adder at all as they claimed.

From Table V, it is seen that the proposed adders consume less power compared to the others. But the proposed 10T adder shows better performance in terms of power consumption (figure 6). On the other hand, the total average delay of the proposed adders is slightly higher than the rest of the adders (figure 7). In terms of delay the proposed circuits performed slightly worse than other two models.

Power delay product (PDP) is another important parameter of any VLSI circuit. The design goal is to minimize PDP, in order to get low power in high frequencies. PDP is also depending on supply power V_{DD}. The proposed adder circuits have lower PDP than other two adders (figure 8). So, it is obvious that the proposed circuits are more energy efficient. In order to reduce the PDP, one can reduce the V_{DD}, however, delay is inversely proportional to the V_{DD}. For that reason, the proposed circuit has greater delay. The required silicon area is calculated from the layout designed by Cadence virtuoso tool using 45nm technology. The results are depicted in Table VI. It is observed that the proposed 8T adder circuit needs almost half (57.14 μm^2) of the area as compared with the recently proposed model [2].

TABLE VI. SILICON AREA FOR DIFFERENT ADDERS

SL.NO	*Adder Name*	*Area (μm^2)*
1	Proposed 8T Adder	57.143
2	Reddy 6T Adder (With Inverter)	101.644

VII. CONCLUSION

The addition is one of the basic arithmetic operations which is used in many VLSI applications. So, an efficient adder circuit is necessary for improving the overall performance of other electronic circuits which are embedded in the adder unit. In this research, two new adder models are proposed. Those are simulated extensively considering all practical aspects. Transistors of 16nm low power high k strained silicon model are used to get nearly close practical data. Most basic parameters of the proposed circuits are calculated and compared to other existing efficient adder circuits. In terms of compactness and power efficiency, the proposed adders are superior to others. But the total average delay of the proposed circuits is slightly higher. By considering the trade-off between the power consumption and total delay, the proposed circuits perform better.

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