Analytical formulas and measurement technique for the built-in potential of practical semiconductor junctions

Miron Cristea Electronics, Telecommunication and Technology Information Faculty University Politehnica of Bucharest Bucharest, Romania miron.cristea@ieee.org

Abstract— Based on Gauss' law for the electric field, new formulas were deduced, that enable for the first time the writing of an analytical formula of the built-in potential of implanted and diffused semiconductor junctions. Consequently, in this work is devised a measurement technique for the built-in potential of such junctions. Such measurement is useful because new semiconductor materials besides silicon are more and more used today, like silicon-carbide (SiC) and gallium-nitride (GaN), which have larger bandgap and junction built-in potential. Finding the built-in potential helps adjusting the computer assisted design (CAD) tools and validates the simulation of such wide-bandgap devices.

Keywords— built-in potential, implanted, diffused junctions, space-charge region, electric field, barrier capacitance, measurement technique

I. INTRODUCTION

Today, more and more are used new semiconductor materials besides silicon, like silicon-carbide (SiC) and gallium-nitride (GaN) which have larger bandgap and junction built-in potential. Knowing the built-in potential of the junctions of such devices helps in adjusting (calibrating) the computer assisted design (CAD) tools of such materials and validates the simulation of these devices, therefore finding its value is desirable.

Although the value of the built-in potential of step junctions is easily calculated from the two values of the doping on each side of the junction with a simple, well-known formula, same calculation for highly asymmetrical, implanted or diffused junctions is more complicated. Some researchers approximate its value with the open-circuit voltage of solar cells [1] or use general-physics simulation software (which is very time consuming) to determine it [2], while stating it is one of the "several critical parameters" of such devices [3] and "difficult to detect directly"[4].

Based on Gauss' law for the electric field, new formulas were deduced, with applications to semiconductor junctions [5]. They enable for the first time the writing of analytical formulas for the built-in potential and consequently the devising of a measurement technique for implanted and diffused semiconductor junctions. II. THEORY

A. The New Physics Formula

Gauss' law for the electric field over an electrically charged space region is [6,7]:

$$\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon} \tag{1}$$

where *E* is the electric field, ρ is the electric space charge density and ε the electrical permittivity. One-dimensional case is assumed, also linear, non-dispersive material.

The electric field E relates to the electric potential u in accordance with [6, 7]:

$$E = -\frac{du}{dx} \tag{2}$$

By writing (1) as

$$dE = \frac{\rho(x)}{\varepsilon} dx \tag{3}$$

multiplying the equation by x, and taking into consideration that

$$d(xE) = xdE + Edx \tag{4}$$

the next equation is obtained [5]:

$$\frac{x\rho(x)}{\varepsilon}dx = d(xE) - Edx$$
(5)

The integration of (5) over the space charge region (SCR) – the region with electric charge density ρ – gives:

$$\int_{x_{1}}^{x_{2}} \frac{x\rho(x)}{\varepsilon} dx = \int_{x_{1}}^{x_{2}} d(xE) - \int_{x_{1}}^{x_{2}} E dx \qquad (6)$$

with x_1 and x_2 the limits of the SCR.

Taking (2) into account, then:

$$\int_{x_1}^{x_2} \frac{x\rho(x)}{\varepsilon} dx = \int_{x_1}^{x_2} d(xE) + \int_{x_1}^{x_2} du$$
 (7)

and by integration in the right hand of this equation:

$$\int_{x_1}^{x_2} \frac{x\rho(x)}{\varepsilon} dx = x_2 E(x_2) - x_1 E(x_1) + u(x_2) - u(x_1)$$
(8)

B. Particularization to Semiconductor Junctions

In the case of semiconductor junctions, since the electric field is zero at both ends of the SCR [7, 9], the first two terms in the right hand of (8) vanish, and the next equation is obtained:

$$\int_{x_1}^{x_2} \frac{x\rho(x)}{\varepsilon} dx = V_{SCR}$$
(9)

where V_{SCR} is the total voltage drop across the space charge region. In case of reverse biasing the junction:

$$V_{SCR} = V_{bi} + V_R \tag{10}$$

with V_{bi} the built-in potential of the junction and V_R the applied reverse voltage. In case of forward applied bias:

$$V_{SCR} = V_{bi} - V_F \tag{11}$$

with V_F the applied forward voltage.

III. THE FORMULA OF THE BUILT-IN POTENTIAL

In the case of a semiconductor junction without external bias, V_{SCR} equals the built-in potential of the junction V_{bi} :

$$V_{bi} = \int_{x_1}^{x_2} \frac{x\rho(x)}{\varepsilon} dx$$
(12)

A. Assymetrical, Gaussian profile junctions

In this case, the goal is to calculate the built-in potential of a diffused or implanted junction with lower side doping that approximately follows a Gaussian profile – Fig1. For such junctions, the impurity profile is given by:

$$N_d(x) = N_0 exp\left(-\frac{x^2}{L_d^2}\right)$$
(13)

where N_0 is the maximum concentration and L_d is the technological diffusion length [7,8]:



Fig. 1. Doping profile of a hyper-abrupt p-n junction. X_j is the junction coordinate and x_s the coordinate of the semiconductor surface.

$$L_d = 2\sqrt{D_i t_d} \tag{14}$$

with D_i - the doping impurity diffusion constant at certain diffusion temperature and t_d the diffusion time.

Accordingly, in the depletion approximation, the space charge density is:

$$\rho(x) = qN_d(x) = qN_0 exp\left(-\frac{x^2}{L_d^2}\right) \qquad (15)$$

where q is the elementary electric charge.

Inserting (15) into (12) and integrating the Gaussian profile with $x_1 = 0$ (junction is asymmetric, formed at maximum profile concentration of the lower doped side) and $x_2 = W_{SC0}$ - the depletion region width of the junction at no external bias, the following relation is obtained:

$$V_{bi} = \frac{qN_0L_d^2}{2\varepsilon} \left[1 - exp\left(-\frac{W_{SC0}^2}{L_d^2}\right) \right]$$
(16)

Since the zero-bias barrier capacitance per unit area of a junction is given by [7-9]:

$$C_{b0} = \frac{\varepsilon}{W_{SC0}} \tag{17}$$

results:

$$V_{bi} = \frac{qN_0L_d^2}{2\varepsilon} \left[1 - exp\left(-\frac{\varepsilon^2}{L_d^2 C_{b0}^2}\right) \right]$$
(18)

This formula gives the possibility of determining the built-in voltage by measurements of the barrier-capacitance of the junction.

In the case the junction is also reverse biased, (18) becomes:

$$V_{bi} = \frac{qN_0L_d^2}{2\varepsilon} \left[1 - exp\left(-\frac{\varepsilon^2}{L_d^2C_b^2}\right) \right] - V_R \quad (19)$$

Notice that C_{b0} has been replaced with C_b , the junction barrier capacitance at the reverse bias V_R .

This formula makes possible to determine V_{bi} from measurements of the barrier capacitance at various reverse voltages. It is similar, but different from the "classic" formula of S.M. Sze's book [8] – page 187, equation 45 and observation following:

$${}^{"}C(V) = \left(\frac{q\epsilon_s}{2}C_B\right)^{1/2} \left(V_{bi} + V_R - \frac{2kT}{q}\right)^{-1/2}$$
$$= \frac{\epsilon_s}{\sqrt{2}L_D} (\beta V_{bi} + \beta V_R - 2)^{-1/2}$$
(45)

where C_B is the substrate doping concentration, $\beta \equiv q/kT$, and

 L_D = the Debye length = $\left(\frac{\epsilon_s}{qC_B}\frac{kT}{q}\right)^{1/2}$ (46) Thus, V_{bi} can be determined from the junction capacitance at zero reverse bias from Eq.45".

The new formula presented here is more accurate, because in the inference of the classic one it was supposed that the lower doping concentration of the junction is constant, which is not the actual situation (see (13) and Fig.1).

Particular case: we obtain simpler formula than (16) and (19) when $W_{SC} \ll L_d$, (large $C_b \rightarrow C_{b0}$, small $V_R \rightarrow 0$). Formulas (16) and (19) simplify to:

$$V_{bi} = \frac{qN_0\varepsilon}{2C_{b0}^2} = \frac{qN_0W_{SC0}^2}{2\varepsilon}$$
(20)

because for small x:

$$exp(-x^2) \cong 1 - x^2 \tag{21}$$

IV. MEASURING THE BUILT-IN POTENTIAL

According to (18) and (20), the determination of the builtin potential of the junction is accomplished by the measurement of the zero-bias barrier capacitance. This can be made with simpler circuits or using a dedicated C-V Measurement Parameter Analyzer. In this last case, (19) will be used together with the capacitance vs. voltage sweep data. If the maximum concentration N_0 is known from another measurement (like spreading resistance measurement), then (19) will give a V_{bi} value for each $C_b - V_R$ pair. In this case, an average value for the built-in potential will be the result. Alternatively, the $C_b(V_R)$ curve can be used to infer both values, for V_{bi} and N_0 by a parameter extraction calculation in (19).

A. Experimental

In Table I are presented measured values of the barrier capacitance C_b versus the reverse applied voltage V_R over the p-n junction. They are depicted in Fig. 2, as the function $1/C_b^2$

versus V_R , which is the customary way to determine the builtin potential of step, constant doping junctions [8].

TABLE I.	MEASURED CAPACITANCE VS. VOLTAGE VALUES FOR A
	BB135 VARICAP DIODE

$V_R(V)$	$C_b(pF)$
0.5	19
2	13
4	9
6	7
7	6
9	5

It is noteworthy that the experimental points dependence cannot be approximated by a straight line, the best fit being a quadratic function, so the classic way of finding the built-in potential, by extrapolating the straight line to the intersection with X axis, does not work in this case.

B. Numerical fit and V_{bi} extraction

Consequently, (19) was used to fit the experimental data and extract the value of the built-in potential, Fig. 3.

The resulted value is $V_{bi} = 404 \text{ mV}$, which corresponds with a low doped p-n junction like in Fig. 1, at about 10^{14} cm^{-3} . Lower doping allows a greater variation of the capacitance with applied voltage. The confidence factor of the fit is $R^2 =$ 0.978. The distance from the ideal value of 1 indicates some distortion of the Gaussian profile, most likely due to fieldassisted diffusion – [8] page 194.



Fig. 2. Classic plot - inverse squared barrier capacitance versus reverse applied voltage of the p-n junction in Table I.

Observation: sometimes it is used the next formula for fitting the barrier capacitance, derived from the formulas of the barrier capacitance of abrupt-asymmetric and linear junctions:

$$C_b = \frac{C_{b0}}{\left(1 + \frac{V_R}{V_{bi}}\right)^m} \tag{22}$$

where m = 0.5 for abrupt (with constant doping concentrations on both sides of the junction) and 0.333 for linear junctions.

Trying a fit of the values in Table I using (22) results V_{bi} = 3.27 V, clearly a too large value.



Fig. 3. Plot of barrier capacitance versus reverse applied voltage of the p-n junction in Table I.

CONCLUSIONS

Based on Gauss' law for the electric field, a new physics formula was deduced, together with one of its possible applications - analytical formulas for the built-in potential of implanted and diffused semiconductor junctions. The measurement technique for the determination of the built-in potential of these junctions was devised, such a measurement being useful e.g. for adjusting/calibrating the computer assisted design (CAD) tools of wide bandgap materials and to validate the simulation of wide bandgap semiconductor devices.

The application of the measurement technique on a varicap diode shows a good fit with the experimental data and provides the corresponding value of the junction built-in potential.

This method is much easier to use than a full generalphysics program simulation and applies also when the classic determinations used for constant-concentration or linear junctions prove not suitable.

References

- M. Mingebacha, C. Deibelb, "Built-in potential and validity of Mott– Schottky analysis in organic bulk heterojunction solar cells", Experimental Physics VI, Julius-Maximilians-University of Wurzburg, 2011.
- [2] M. Guo, Y. Li, G. Qin, M. Zhao, "Nonlinear solutions of PN junctions of piezoelectric semiconductors", Acta Mechanica, Vol. 230, Issue 5, May 2019.
- [3] J. Diekmann, P. Caprioglio, D. Rothhardt, M. Arvind, T. Unold, T. Kirchartz, "Pathways towards 30% efficient single-junction perovskite solar cells", ResearchGate preprint, Oct. 2019.
- [4] Chenming Hu, "Modern Semiconductor Devices for Integrated Circuits", pg.92, Prentice Hall, 2010
- [5] M.J. Cristea, "Calculation of the depletion region width and barrier capacitance of diffused semiconductor junctions with application to reach-through breakdown voltage of semiconductor devices with diffused base", International Semiconductor Conference, IEEE-CAS, Sinaia, Romania, 2007.
- [6] Bo Thide, "Electromagnetic field theory", Upsilon Books, Uppsala, Sweden, 2004.
- [7] A.S. Grove, "Physics and technology of semiconductor devices", Wiley, New York, 1967.
- [8] S.M. Sze, "VLSI technology", McGraw-Hill, New York, 1983.
- [9] S.M. Sze, Kwok Ng, "Physics of Semiconductor Devices", third ed., Wiley, New York, 2007.